UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,563	03/17/2004	Hong Yu Yu	NUS03-001	3494

7590 04/03/2007

STEPHEN B. ACKERMAN
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

EXAMINER	
KIM, SU C	
ART UNIT	**PAPER NUMBER**
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,563	YU ET AL.	
	Examiner	Art Unit	
	Su C. Kim	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-12,14-24,26,27,35,37-43,45-47,54-56,58 and 59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-12,14-24,26,27,35,37-43,45-47,54-56,58 and 59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 13,38,45,50, & 57 is withdrawn in view of the newly discovered reference(s) to Cunningham (US20010013600) and Lim et al.(US20040266204) Rejections based on the newly cited reference(s) follow.

Claim Objections

2. Claim 8 & 24 are objected to because of the following informalities: "a method for fabricating a CMOS semiconductor device structure comprising gate electrodes comprising". Claim language is not clear. The examiner suggests that " - - structure including gate electrodes comprising - -"

Claim 24 is objected to because of the following informalities: " - -gatge electrode - -". Typographical error.

Claim 26 is objected to because of the following informalities: "the second metal layer" is not claimed in claim 24. Please change "the second metal layer" as "the second metal capping layer" for the purpose of consistency. Now the examiner considers the second metal layer as the second metal capping layer.

Claim 40 is objected to because of the following informalities:"- - a hafnium nitride second metal capping layer". Change "- - a hafnium nitride second metal capping layer" as "- - a hafnium nitride being second metal capping layer" or like.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Cunningham (US20010013600).

Pertaining claim 8, Cunningham discloses a method for fabricating a CMOS (Paragraph 0004) semiconductor device structure comprising gate electrodes 140 (Fig. 3a) comprising:

providing a dielectric layer (Fig. 3B, Note: gate dielectric layer is located below 142) on a substrate; depositing a hafnium nitride layer 140 (pargarph 0049) overlying said dielectric layer wherein an atomic ratio of Nitrogen and Hafnium of said hafnium nitride layer is adjusted to adjust the work-function of said gate electrodes (Note: HfN as metal layer 140 has atomic ratio of 1:1) wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one (Note: atomic ratio of HfN is equal to 1 as its stoichiometry);

depositing a capping layer 144 (Fig. 3b, Note: silicon nitride) overlying said hafnium nitride layer 140 (Fig. 3b);

patterning said hafnium nitride layer 140 and said capping layer 144 (Fig. 3b) and said dielectric layer (Note: below 142) to form said CMOS gate electrodes; and forming source and drain regions (paragraph 0018) within said substrate adjacent to said CMOS gate electrodes(Fig. 3b).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 9-10, 24, 40, 41, 43, & 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cunningham (US20010013600) in view Hayashi et al. (US20040157473).**

Pertaining claim 9, as applied to claim 8, Cunningham discloses all the limitations including, depositing of said hafnium nitride layer 140 (Fig 3b).

Cunningham fails to teach flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target.

However, Hayashi discloses flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target (paragraph 0082, lines14-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Cunningham with flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target as taught by Hayashi in order to produce uniform thickness of HfN layer.

Pertaining 10, as applied to claim 9, Cunningham and Hayashi in combination disclose all the limitations including, argon and nitrogen flow (paragraph 0082, lines14-20).

Cunningham and Hayashi in combination fail to teach argon and nitrogen flow rates are kept as constant at 25 sccm and 5 sccm, respectively.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 24- rejected under 35 U.S.C. 103(a) as being unpatentable over Cunningham (US20010013600) in view of Hayashi et al. (US20040157473).

Pertaining claim 24, Cunningham discloses a method for fabricating a CMOS semiconductor device structure 140 (Fig. 3a) comprising gate electrodes comprising:

providing a dielectric layer (Fig. 3B, Note: gate dielectric layer is located below 142) on a substrate;

depositing a first metal layer 140 (pargarph 0049) overlying said dielectric layer depositing a second metal capping layer 144 (Fig. 3b, Note: silicon nitride) overlying said first metal layer 140 wherein said second metal is different from said first metal

patterning said second metal capping layer 144, said first metal layer and said dielectric layer(Fig. 2) to form said CMOS gate electrodes; and forming source and drain regions (paragraph 0018) within said substrate (Fig. 2) adjacent to said CMOS gate electrodes and depositing of said first metal layer140 (Fig. 3b) comprises an atomic ratio of Nitrogen and Hafnium of said hafnium nitride layer is adjusted to adjust the work-function of said gate electrodes (Note: HfN as metal layer 140 has atomic ratio of 1:1) wherein said atomic ratio of nitrogen to hafnium remains greater than or equal to one (Note: atomic ratio of HfN is equal to 1 as its stoichiometry).

Cunningham fails to teach depositing of said first metal layer comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target to form a hafnium nitride first metal laver.

However, Hayashi discloses flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target (paragraph 0082, lines14-20) target to form a hafnium nitride first metal laver.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Cunningham with flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target as taught by Hayashi in order to produce uniform thickness of HfN layer.

Regarding claim 40, Cunningham and Hayashi in combination a method for fabricating a CMOS semiconductor device structure comprising:

providing a dielectric layer (Cunningham, Fig. 3B, Note: gate dielectric layer is located below 142) on a substrate; depositing a first metal layer overlying said dielectric layer;

depositing a second metal capping layer overlying said first metal layer140 (Cunningham, paragraph 0049) wherein said depositing comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target(Hayashi, paragraph 0082, lines14-20) to form a hafnium nitride second metal capping layer;

patterning said first layer 144 and said the second capping layer 114 (Cunningham, Fig. 3b) and said dielectric layer (Cunningham, Fig. 4) to form CMOS gate electrodes (Fig. 3b);

forming source and drain regions within said substrate adjacent to said CMOS gate electrodes (Cunningham, paragraph 0005).

Pertaining claim 41, as applied to claim 40, Cunningham, Hayashi in combination disclose all the limitations including, the dielectric layer comprises HfO_2 (Hayashi, paragraph 0065 & 0068, note: silicon oxide gate insulating layer is replaced by Hafnium Oxide).

Pertaining claim 43, as applied to claim 40, Cunningham, and Hayashi in combination disclose all the limitations including, the first metal layer comprises tungsten or tantalum nitride (Hayashi, paragraph 004).

Pertaining claim 45, as applied to claim 40, Cunningham, and Hayashi in combination disclose all the limitations including, adjusting the flow rate of Nitrogen and Argon atoms to adjust the work-function of said gate electrodes (paragraph 0082, lines14-20) wherein the atomic ration of nitrogen to hafnium remains greater than or equal to one (Note: atomic ratio of HfN is equal to 1 as its stoichiometry).
Pertaining claim 54, as applied to claim 24, Cunningham and Hayashi in combination disclose all the limitations including, argon and nitrogen flow (paragraph 0082, lines14-20).

Cunningham and Hayashi in combination fail to teach flow rates are kept as constant at 25 sccm and 5sccm, respectively.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

8. Claims 11 & 55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cunningham (US20010013600) in view of Hayashi et al. (US20040157473) and Kubota et al. (US20040087124).

Pertaining claims 11 & 55, as applied to claims 8 & 24, Cunningham and Hayashi in combination disclose all the limitations including, said dielectric layer comprises HfO_2 (Cunningham, 0031) and is deposited at 400°C (Hayashi, paragraph 0065 & 0068, note: silicon oxide gate insulating layer is replaced by Hafnium Oxide)

Cunningham and Hayashi in combination fail to teach dielectric HfO_2 using a MOCVD cluster tool.

However, Kubota discloses HfO_2 using a MOCVD cluster tool (Paragraph 0019).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Cunningham and Hayashi in combination with HfO_2using a MOCVD cluster tool as taught by Kubota in order to produce thin dielectric layer.

9. Claims 12 & 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cunningham (US20010013600) in view of Hayashi et al. (US20040157473) and Yeo et al. (US 20040129995).

Pertaining claims 12 & 56, as applied to claims 8 & 24, Cunningham and Hayashi in combination disclose all the limitations including, said dielectric layer comprises HfO2(Hayashi, paragraph 0002).

Cunningham and Hayashi in combination fail to teach the dielectric layer is subjected to post-deposition annealing (PDA) at 700°C in a N2 ambient.

However, Yeo disclose a post-deposition annealing up to 900 degrees Celsius in nitrogen ambient (Paragraph 0029).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Cunningham and Hayashi in combination with a post-deposition annealing up to 900 degrees Celsius in nitrogen ambient as taught by Yeo in order to form better quality dielectric layer.

Cunningham, Hayashi, and Yeo in combination fail to teach the post-depostion annealing at 700 °C.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

10. **Claims 14, 15, 58, & 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cunningham (US20010013600) in view of Haukka et al. (US 6858524).**

Pertaining claims 14 & 58, as applied to claims 8 & 24, Cunningham discloses Hafnium nitride layer 140 (Cunningham, Fig. 3b).

Cunningham fails to teach impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

Haukka discloses impurity doping into said hanium nitride layer (column 8, lines 52-62, metal nitride layer is treated with hydrogen plasma) to tune the work-function of said gate electrodes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Cunningham reference with impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes as taught by Haukka in order to reduce the resistivity of gate electrode.

Pertaining claims 15 & 59, as applied to claims 8 & 24, Cunningham and Haukka in combination disclose thermal treatment of hafnium nitride layer by RTA (Column 8, lines 56-59).

Cunningham and Haukka in combination fail to teach thermal treatment of hafnium nitride layer at about 1000°C for about 20 second.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

11. Claims 26-27, 35, 37, & 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cunningham (US20010013600) in view of Hayashi et al. (US20040157473) and Lim et al. (US20040266204).

Regarding claim 26, as applied to claim 24, Cunningham and Hayashi in combination disclose all the limitations including, said second metal layer

Cunningham and Hayashi in combination fail to teach the second metal capping layer comprises tungsten or tantalum nitride.

Lim discloses the second metal capping layer comprises tungsten or tantalum nitride 24 (Fig. 4D, paragraph 0034 Note: barrier layer 24 can be TaN).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Cunningham and Hayashi in combination with the second metal capping layer comprises tungsten or tantalum nitride as taught by Lim in order to prevent diffusion.

Regarding claim 27, as applied to claim 24, Cunningham, Hayashi, and Lim in combination disclose the first (Hayashi, 0051, CVD (chemical vapor deposition) and second metal layers (Lim, paragraph 004) are deposited by physical vapor deposition or chemical vapor deposition.

Pertaining claim 35, Cunningham, Hayashi, and Lim in combination a method for fabricating a CMOS semiconductor device structure (Cunningham, Paragraph 0004) comprising:

providing a dielectric layer (Cunningham, Fig. 3B, Note: gate dielectric layer is located below 142) on a substrate; depositing a hafnium nitride layer 140 (Cunningham,

paragraph 0049) overlying said dielectric layer wherein said depositing comprises flowing Nitrogen and Argon atoms into a chamber simultaneously wherein said chamber contains said substrate and a hafnium target(Hayashi, paragraph 0082, lines14-20);

depositing a titanium nitride or tungsten capping layer overlying said hafnium nitride layer24 (Lim, Fig. 4D, paragraph 0034 Note: barrier layer 24 can be TaN);

patterning said hafnium nitride layer 144 and said capping layer 114 (Cunningham, Fig. 3b) and said dielectric layer (Cunningham, Fig. 4) to form CMOS gate electrodes (Fig. 3b); and

forming source and drain regions within said substrate adjacent to said CMOS gate electrodes (Cunningham, paragraph 0005).

Regarding claim 37, as applied to claim 35, Cunningham, Hayashi, and Lim in combination disclose all the limitations including, said dielectric layer (Lim, 22) comprises HfO2, silicon dioxide (Lim, paragraph 0034), silicon nitride, nitrided silicon dioxide, zirconium oxide, aluminum oxide, tantalum pentoxide, barium strontium titanates, or crystalline oxides.

Regarding claim 38, as applied to claim 35 Cunningham, Hayashi, and Lim in combination disclose all the limitations including, adjusting the Nitrogen flow (Hayashi, paragraph 0082) rate to adjust the work-function of said gate electrodes wherein the atomic ratio of nitrogen to hafnium in said hafnium nitride layer remains greater than or equal to one (Note: atomic ratio of HfN is equal to 1 as its stoichiometry).

12. Claims 39 & 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cunningham (US20010013600) in view of Hayashi et al. (US20040157473) and Lim et al. (US20040266204) and further in view of Haukka et al. (US 6858524).

Pertaining claim 39, as applied to claim 35, Cunningham, Hayashi, and Lim in combination disclose Hafnium nitride layer 140 (Cunningham, Fig. 3b).

Cunningham, Hayashi, and Lim in combination fail to teach impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

Haukka discloses impurity doping into said hanium nitride layer (column 8, lines 52-62, metal nitride layer is treated with hydrogen plasma) to tune the work-function of said gate electrodes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Cunningham reference with impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes as taught by Haukka in order to reduce the resistivity of gate electrode.

Pertaining clam 42, as applied to claim 40, Cunningham, Hayashi, and Lim in combination disclose all the limitations including, the first (Hayashi, 0051, CVD (chemical vapor deposition) and second metal layers (Lim, paragraph 004) are deposited by PVD or CVD.

13. **Claims 46 & 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cunningham (US20010013600) in view of Hayashi et al. (US20040157473) and Haukka et al. (US 6858524).**

Pertaining claim 46, as applied to claim 40, Cunningham, and Hayashi in combination disclose Hafnium nitride layer 140 (Cunningham, Fig. 3b).

Cunningham, and Hayashi in combination fails to teach impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes.

Haukka discloses impurity doping into said hanium nitride layer (column 8, lines 52-62, metal nitride layer is treated with hydrogen plasma) to tune the work-function of said gate electrodes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Cunningham reference with impurity doping into said hafnium nitride layer to tune the work-function of said gate electrodes as taught by Haukka in order to reduce the resistivity of gate electrode.

Pertaining claim 47, as applied to claim 40, Cunningham, Hayashi, and Haukka in combination disclose all the limitations including, thermal treatment of hafnium nitride layer by RTA (Haukka, column 8, lines 56-59).

Response to Arguments

14. Applicant's arguments with respect to claims 8-12, 14-24, 26-27, 35, 37-43, 45-47, 54-56, & 58-59 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Su C. Kim whose telephone number is (571) 272-5972. The examiner can normally be reached on Monday - Thursday, 9:00AM to 7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Su C. Kim (3/23/2007)

W. David Coleman
Primary Examiner